Performance Comparison for A4WP Class-3 Wireless Power Compliance between eGaN® FET and MOSFET in a ZVS Class D Amplifier

Michael de Rooij, Efficient Power Conversion, 909 N. Sepulveda Blvd. ste230, El Segundo CA, 90245, U.S.A., Michael.derooij@epc-co.com

Abstract

eGaN FETs have repeatedly demonstrated higher efficiency than MOSFETs in wireless power transfer amplifiers when operated over a wide impedance range using a ZVS Class D amplifier [1, 2, 3, 4, 5, 6, 7, and 8]. In this article we examine a method to further improve the performance of eGaN FETs by replacing the bootstrap diode of the high side gate driver with an eGaN FET that is driven synchronously with the lower device gate. The integrated bootstrap diode of the gate driver has reverse recovery losses (P_{QRR}), as it is very difficult to monolithically integrate a Schottky diode on the same wafer as the gate driver circuit. This limits high frequency performance of the amplifier because the frequency dependent reverse recovery losses are dissipated in the upper device. The technique that replaces the internal bootstrap diode of the gate driver will be implemented and evaluated using an eGaN FET based ZVS Class D amplifier and compared to an equivalent MOSFET version operated over a wide load impedance range of ±35j Ω to the A4WP Class-3 drive specifications [9]. The results show that the eGaN FET based amplifier losses were reduced between 15% and 48%, and it could operate over a wider load impedance range, by as much as 20j Ω, than the comparable best-in-class MOSFET amplifier.

1. Introduction

Wireless energy transfer solutions, driven by the desire for convenience-of-use and extended battery life, have contributed to emerging standards such as the Alliance for Wireless Power (A4WP) [9, 10], also known as rezence™. The A4WP standard operating at 6.78 MHz is the only wireless power standard to truly address convenience-of-use issues such as source to device distance, device orientation on the source, multiple devices on a single source, higher power capability, simplicity of use, and imperfect placement. To address the convenience-of-use, the amplifier needs to drive a wide impedance load range of the source coil. This wide impedance load range together with the A4WP Class-3 drive requirements will serve as a foundation to which the amplifier will be tested. The goal is to determine the maximum imaginary load range that the amplifier can drive to the specifications without any component exceeding predetermined specifications such as temperature and voltage limits.

The high-efficiency Class E topology [1, 11, and 12] has received a lot of attention as a suitable amplifier for a wireless energy transfer; however, load impedance variations impacting the operating point have made the design difficult and complex. Unlike the Class E amplifier, the impact of load impedance variations on the ZVS Class D amplifier [1, 4, 5, and 7] is less severe. eGaN FETs have already been proven to yield superior performance and higher efficiencies in the ZVS Class D topology than MOSFETs. However, the internal bootstrap diode of the gate driver still presents a limiting factor to performance. It is currently not possible to monolithically integrate the required Schottky diode into the gate driver and hence this diode will have reverse recovery losses. These losses are induced into the upper device of the Class D topology and are proportional to both supply voltage and frequency. In this paper we examine a method to eliminate the reverse recovery losses of this diode and

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re-examine the performance of the ZVS Class D amplifier when driving a wide impedance load.

2. The ZVS Class D Amplifier

The ZVS Class D amplifier was chosen over other amplifiers as it demonstrates superior performance when fitted with eGaN FETs [1, 4, 5, and 7]. The basic schematic of the ZVS voltage mode Class D amplifier shown in Fig. 1 (left) and is comprised of three main components; (1) a half bridge switching converter (Q_1 and Q_2), (2) a ZVS tank circuit (L_{ZVS} and C_{ZVS}), and (3) a resonant load (Z_{load} & C_s). The load impedance Z_{load} represents the equivalent impedance of the entire coil set that includes the device coil, coupling, device matching, rectifier, and DC load resistance. Also shown in Fig. 1 (right) are various waveforms for the amplifier operating under ideal conditions.

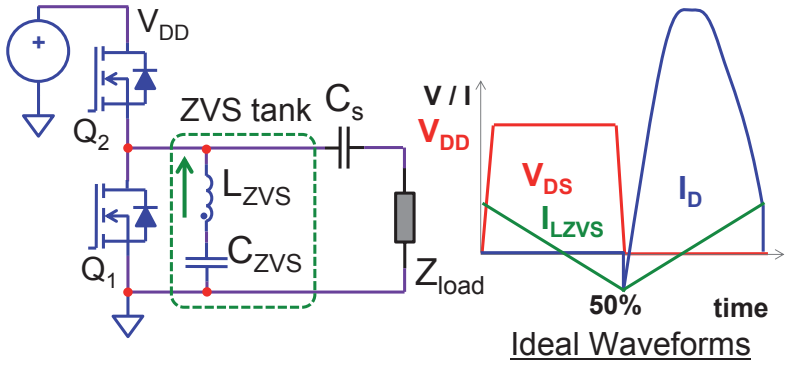

Fig. 1. ZVS Class D amplifier with ideal operating waveforms.

2.1. Device Selection and Comparison

The ZVS Class D amplifier must be capable of driving an impedance load range of ±35j Ω and 1.7 Ω through 57 Ω while delivering 800 mA which is derated once the power delivered reaches 16 W. At the extreme impedances of 57 Ω ±35j Ω, the load requires an output voltage of at least 32.3 V. Since the voltage gain (DC to AC_{RMS}) of the ZVS Class D amplifier is 0.45 [8, 13], a supply voltage of at least 72 V for a single ended configuration is needed. Accounting for experimental variations, a full supply voltage of 80 V is chosen to drive the load at the extreme impedances. Allowing for a voltage margin of 20%, 100 V minimum rated devices should be used for the design.

The magnitude of C_{OSS} is an important factor in the design of the ZVS Class D amplifier, where smaller is better, and hence the smallest 100 V rated eGaN FET, the EPC8010 [14] with $R_{DS(on)}$ of 125 mΩ, was chosen for experimental evaluation. An equivalent best-in-class MOSFET, the FDMC86116LZ [15] with $R_{DS(on)}$ of 100 mΩ, was chosen for experimental comparison, as it can be driven using a 5 V gate.

A wireless figure of merit (FOM_{WPT}) has previously been defined [7, 12] and is updated for the ZVS Class D topology and used to compare the selected devices. The traditional FOM [16] is derived by multiplying the voltage transition gate charge (Q_{GD}) with the on-state resistance ($R_{DS(on)}$) of the device, but since the ZVS Class D is zero voltage switching, the voltage transition portion of the gate charge (Q_{GD}) becomes negligible. In this case, the total gate charge (Q_G) minus the voltage transition portion (Q_{GD}) is used instead [7, 12].

Despite the voltage across the output capacitance (C_{OSS}) of the devices being transitioned by the ZVS tank circuit current (I_{ZVS}), it is still an important factor in device selection as it drives

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losses when the load is off resonance. In particular, capacitive loads can rapidly lead to high C_{OSS} losses when the effect of the ZVS tank current has been negated by the load current and the circuit becomes hard-switching.

Based on these factors an updated wireless power transfer figure of merit can be defined using equation-1.

$$FOM_{WPT} = R_{DS(on)} \cdot (Q_G - Q_{GD} + Q_{OSS}) \quad (1)$$

Where: Q_{OSS} = Output capacitance charge [C]

Device reverse recovery (Q_{RR}) has been excluded from FOM_{WPT} as it is only defined for one condition in the MOSFET datasheet and the eGaN FET has no Q_{RR} making it difficult to use a reliable value for comparison. Therefore any value of reverse recovery for the MOSFET yields additional losses whereas the eGaN FET will remain at zero.

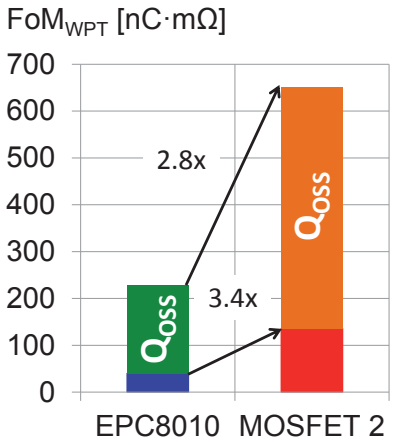

Fig. 2. FOM_{WPT} comparison between the EPC8010 [14] and best-in-class MOSFET [15].

Using the updated FOM_{WPT} the two devices selected for evaluation can be compared and is shown in Fig. 2 where a lower value indicates a superior device. Both the gate charge and output capacitance components are lower for the eGaN FET than the MOSFET by a factor of 3.4 and 2.8 respectively.

The selected MOSFET is available in a 3 mm x 3 mm micro lead-frame package (MLP) and the eGaN FET as a 2 mm x 0.85 mm land grid array (LGA) wafer level package (WLP). The difference in device PCB area between the selected eGaN FET (3.5 mm^2) and MOSFET (18 mm^2) is 5 times and represents a 40 % reduction in total amplifier area that includes the gate driver and ZVS tank circuit.

3. Gate Driver Reverse Recovery Losses

The 100 V capable LM5113 gate driver was used to drive the half bridge eGaN FET topology. Using a technique named voltage clamping [17, 18], the carefully designed gate driver ensures that the upper device is never exposed to an over-voltage that can occur when the lower device “body diode” conducts current [17, 18]. To achieve this, the bootstrap power supply diode is integrated into the driver, and since it is very difficult to monolithically integrate a Schottky diode on the same wafer, this P/N junction diode has reverse recovery and associated losses (P_{QRR}). This limits high frequency performance of the ZVS Class D amplifier because the frequency dependent reverse recovery losses are dissipated in the upper device. Replacing the internal diode with an external Schottky diode is also not a

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viable solution as the gate driver does not make provision for this and thus cannot prevent an upper device over-voltage if the internal circuitry is bypassed. The reverse recovery losses induced into the upper device can be calculated using equation-2 [18].

$$P_{QRR} = Q_{RR} \cdot V_{DD} \cdot f \qquad (2)$$

Where: P_{QRR} = Reverse recovery losses [W]
Q_{RR} = Reverse recovery charge of the gate driver bootstrap diode [C]
V_{DD} = Supply voltage to the ZVS Class D amplifier [V]
f = Operating frequency [Hz]

The LM5113 gate driver bootstrap diode reverse recovery charge (Q_{RR}) is approximately 2 nC [18] which yields 678 mW of losses induced in the upper device when the ZVS Class D amplifier is operating at 50 V. A method to eliminate these losses from the amplifier without affecting overall performance is needed.

3.1. Implementing the Synchronous FET Bootstrap Supply

To prevent reverse recovery of the internal bootstrap diode requires that it never conducts current; however this also means that since it no longer operates, its function must be replaced. The schematic block diagram of Fig. 3 shows how to achieve this. First an eGaN FET (Q_{BTST}), which has no reverse recovery charge, and of same voltage rating as the main FETs (Q_1 and Q_2), is added to the general gate driver to replace the function of the internal bootstrap diode. Next, the internal bootstrap diode is prevented from conducting current by permanently reverse biasing it. This is achieved by slightly lowering the supply voltage to the gate driver by about 0.3 V. The addition of the bootstrap FET with source connected to the 5 V supply means that the bootstrap voltage across C_{BTST} will be nearly 5 V. The combination of the higher bootstrap voltage and lower gate driver voltage increases the voltage difference across the internal bootstrap diode thus permanently reverse biasing it.

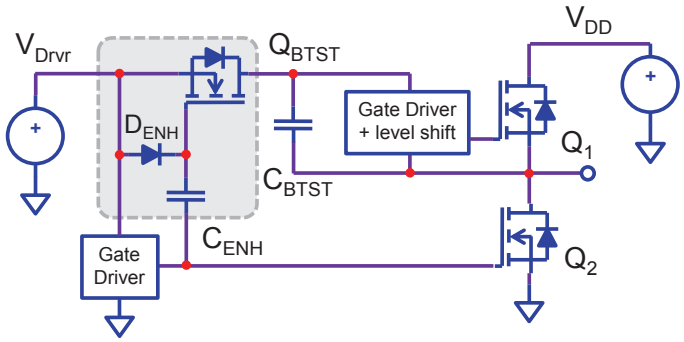

Fig. 3. Schematic implementation of the synchronous FET bootstrap supply.

The bootstrap FET is then driven synchronously with the lower FET (Q_2) which is required to prevent it from conducting and thus charging C_{BTST} when the lower device (Q_2) is conducting a negative current in the off state (“body-diode” mode). Since an eGaN FET is used for Q_{BTST} and is an enhancement mode device with its source is connected to 5 V, the lower gate output voltage needs to be offset by 5V to correctly control the gate of Q_{BTST}. A second bootstrap circuit, comprised of D_{ENH} and C_{ENH}, is used to achieve this using a very small low voltage Schottky diode with no reverse recovery.

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4. Experimental Verification

The ability of the synchronous FET bootstrap supply circuit to improve the performance of the ZVS Class D amplifier will be experimentally verified and again compared with a best-in-class MOSFET equivalent following the same procedure described in [7].

4.1. Experimental Setup

The experimental setup is the same setup as described in [7] and comprises two main components, (1) an amplifier under test, and (2) a discrete programmable load with an adjustment range from 1.7 Ω though 57 Ω and from -35j Ω though +35j Ω. Initially the discrete programmable load, including the oscilloscope current probe, was calibrated using a VNA. The results would be used during the power experiments to accurately determine the RF power delivered by the amplifier. Since there are no non-linear components present in this discrete programmable load, the small signal VNA (+10 dBm) measurements were considered valid for large signal performance during power testing.

Testing commences by setting the imaginary impedance to 0j Ω and the load resistance adjusted over the full range. This test relies on the current and power requirements of the A4WP Class-3 standard. During testing the device and gate driver temperature are monitored to ensure that none exceeded 100°C. In addition, the supply voltage (V_{DD}) to the amplifier was limited to 80 V. If either condition were to be violated then that measurement was regarded as a fail. For each successive pass, the magnitude of the imaginary impedance would be increased until the compliance test failed.

4.2. Experimental Results

The MOSFET version of the amplifier was found to be A4WP Class-3 compliant over the imaginary impedance range of -30j Ω though +20j Ω whereas the eGaN FET version of the amplifier was found to be A4WP Class-3 compliant over the imaginary impedance range of -35j Ω though +35j Ω, a relative difference of 20j Ω. At ±35j Ω the required voltage for the amplifier to drive the coil reached 80 V and is the only limiting factor for the eGaN FET amplifier. In the case of the MOSFET amplifier the gate driver or device temperature exceeding 100°C were the limiting factors.

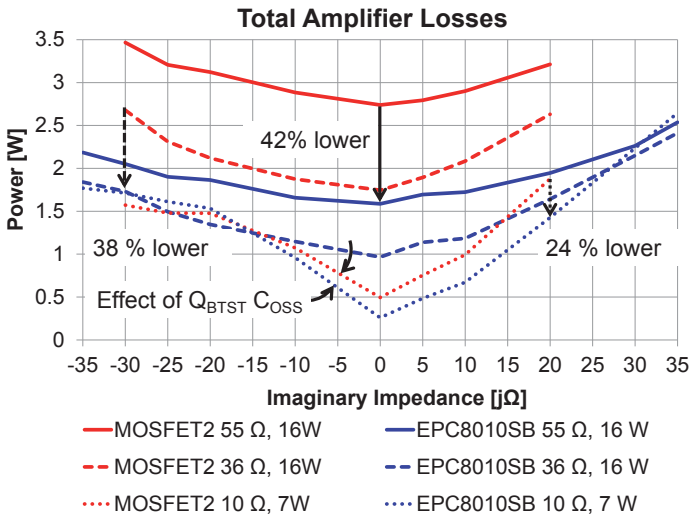

Fig. 4. Experimental comparison between MOSFET (red) and eGaN FET (blue) total amplifier losses as function of imaginary load impedance for various real load impedances.

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Fig. 4 shows the measured total amplifier losses, including the gate driver, as function of imaginary load impedance for various load resistance. The higher the load resistance became the greater the performance benefit the eGaN FET version of the amplifier had over the MOSFET version.

Implementation of the synchronous FET bootstrap power supply required the smallest available 100 V rated eGaN FET. In this case it was the same device used for the main circuit EPC8010 [14] and which is too large for this application. The result was that its C_{OSS} was on the same order of magnitude as the main devices and would contribute to the main power circuit capacitance that is transitioned by the ZVS tank circuit current (I_{ZVS}). This accounts for the decreased performance, evident on Fig. 4, in the capacitive load region (negative impedance) as a portion of the ZVS tank circuit current is used to offset the capacitive load current that is not present without the synchronous FET bootstrap supply implementation. This can easily be overcome once a smaller device with significantly lower output capacitance (C_{OSS}) becomes available.

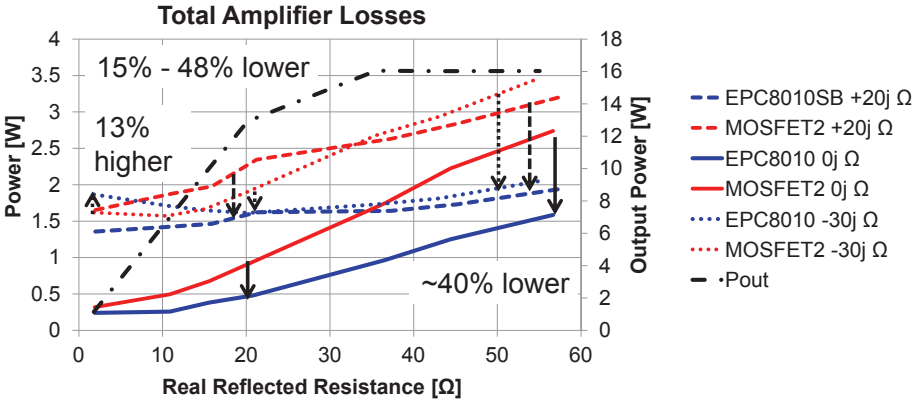

Fig. 5. Experimental comparison between MOSFET (red) and eGaN FET (blue) total amplifier losses as function of load resistance for various imaginary load impedances.

The measured total amplifier power loss for both the eGaN FET and MOSFET based amplifiers operating under a resistance load variation of 1.7 Ω through 57 Ω and for three imaginary impedance load conditions, where both amplifiers were fully A4WP Class-3 compliant, of -30j Ω, 0j Ω, and +20j Ω, is shown in Fig. 5. For the load power range between 6.5 W and 16 W the eGaN FET amplifier has between 15% and 48% lower losses than the MOSFET version. In the power range below 6.5 W the eGaN FET based amplifier maintains lower losses except when the load becomes capacitive, where the difference is small at 13% in the worst case, and is due to the lack of availability of a very small synchronous FET bootstrap with negligible C_{OSS} with respect to the main devices (Q_1 and Q_2).

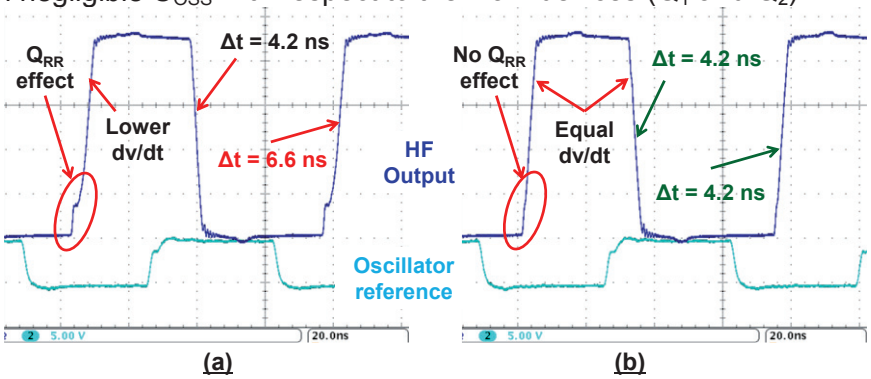

Fig. 6. No load measured waveforms of the amplifier output without the synchronous FET bootstrap implementation (a) and with it (b) when operating at 45 V.

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The benefit of removing the reverse recovery charge of the gate driver can be seen on the waveform of Fig. 6 where without the implementation of the synchronous FET bootstrap supply, the waveform (a) shows a distinctive bump at the onset of the rising edge that is missing when implementing the synchronous FET bootstrap supply (b). This also ensures that the rising edge and falling edge slopes will match after implementation.

5. Conclusions

An experimental evaluation of an eGaN FET and MOSFET based ZVS Class D amplifiers operating over a wide impedance range in compliance with the A4WP Class-3 standard were presented in this paper. The eGaN FET version was fitted with a synchronous FET bootstrap power supply capable of eliminating the reverse recovery losses associated with the internal diode of the gate driver bootstrap circuit. The eGaN FET version yielded between 15% and 48% lower operating losses than a best-in-class MOSFET version and could operate over a wider imaginary impedance load range from -35j Ω through +35j Ω whereas the MOSFET could only achieve -30j Ω through +20j Ω. Testing required that neither the FETs or gate driver temperature was to exceed 100°C or that the voltage needed to drive the amplifier exceed 80 V. In the case of the MOSFET amplifier, thermal limits were reached preventing wider impedance range capability. In the case of the eGaN FET amplifier the maximum supply voltage of 80 V had been attained.

The lower C_{OSS} of the eGaN FET relative to an equivalent MOSFET ensures a lower loss amplifier is possible, even when the devices are hard-switching, such as under highly capacitive load conditions. The lower C_{ISS} also results in lower gate driver power consumption to operate the eGaN FET based amplifier.

Implementation of the synchronous FET bootstrap supply could be achieved without adding an additional gate driver or significantly increasing the complexity of the circuit. Given that these results used a device for the synchronous FET bootstrap supply function that is too large for this application, the benefits can only improve further once a smaller device becomes available.

Space and volume come at a premium for many modern applications. In the case of an eGaN FET based ZVS Class D amplifier suitable for wireless power transfer, a total of a 40% area reduction over an equivalent MOSFET based amplifier can be achieved in addition to all the savings in energy efficiency and system complexity.

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